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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/559,638	12/02/2005	Xiaowu Gong	1890-0330	7260

7590 08/22/2007  
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EXAMINER
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KINKEAD, ARNOLD M

ART UNIT	PAPER NUMBER
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2817

MAIL DATE	DELIVERY MODE
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08/22/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/559,638

Applicant(s)

GONG, XIAOWU

Examiner

Arnold Kinkead

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-17 is/are allowed.
- 6) ☒ Claim(s) 1-3 and 8 is/are rejected.
- 7) ☒ Claim(s) 2-7 and 9 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_.

## DETAILED ACTION

### *Specification*

The abstract of the disclosure is objected to because it should be on a separate page. Correction is required. See MPEP § 608.01(b).

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2,3, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Sauer(US 5,497,127 cited by applicant).

**The reference by Sauer discloses a tunable oscillator, see figure 1, with a control supply(hysteresis circuit(199)) that allows for tuning of the oscillator; The oscillator circuit signal(C1) is shown to be compared with a reference signal(N1) which has an amplitude that varies(See col. 4, line 42-col. 5, line 42):**

"(15) In the circuit 199, a current provided by transistor 187, responsive to the control potential CS1, generates the hysteresis signal N1 through a voltage divider formed by resistors 189, 191 and 195. In this voltage divider, the resistor 195 is selectively shunted by the resistor 185, responsive to the signal DN, or by a combination of the resistor 185 and a resistance through

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transistor 197, which is determined by the level of the control signal CVC0. This selective shunting of the resistor 195 changes the potential N1 which is applied to the differential comparator 175 from a relatively positive potential, when resistor 195 is shunted by the combined resistance of elements 185 and 197 to a relatively negative value when resistor 195 is shunted by resistor 185 alone (i.e. when transistor 198 is conductive).

(16) When the signal DN is in a logic-low state, the transistor 198 is not conductive and the resistance of the voltage divider network is determined by the fixed resistors 189 and 191, the resistance of the resistor 195 in parallel with the resistance of resistor 185 and the variable resistance of transistor 197. As described above, the resistance of transistor 197 varies in inverse proportion to the control signal CVC0.

(17) When signal DN is in a logic-high state, transistor 198 is conductive and the resistance of the voltage divider network is determined as the combined resistance of resistors 189, 191 and the shunt combination of resistors 195 and 185. This significantly reduces the value of the signal N1.

(18) The hysteresis signal N1 is at a relatively high level when capacitor 152 is being charged from a relative negative potential to a relatively positive potential, and at a relatively low level when capacitor 152 is being discharged from a relatively positive potential to a relative negative potential. The output signal of the differential comparator 175 is applied to the differential to single-ended level shifter 183...

(20) Also at time T1, the signal DN renders the transistor 198 conductive, reducing the resistance of the bottom component of the voltage divider which forms the hysteresis circuit 199. This causes the signal N1 to decrease from approximately 2.7 volts to approximately 2.2 volts.

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(21) At time T2, the negative ramp of the signal C1 also reaches 2.2 volts, causing the relative amplitudes the signals A and B to reverse. This reversal is sensed by the circuitry 183 which, in response, causes the signals DN and CLK to change state from positive to negative. Shortly after time T2, signal DN is at ground potential, rendering the transistors 148 and 150 non-conductive. This stops the current drain from capacitor 152, allowing the capacitor to again be charged by the current provided through transistor 136. This results in the positive going slope of the triangle wave C1 between times T2 and T3. The change in state of the signal DN also renders transistor 198 non-conductive, increasing the resistance in the voltage divider network of the hysteresis circuit 199. This increase in the resistance increases the signal N1 from 2.2 volts to 2.7 volts. At time T3, the signal C1 has charged to 2.7 volts and the process begins again as described above with reference to time T1. "

**As described above there is an inverse relationship between the control output passing through the delay compensation(including inverter 192 and hysteresis circuit 199) and the amplitude of the reference signal, N1. The oscillator circuit has a capacitor(152) that is charged and discharged in response to the comparison(via 148,150).**

***Allowable Subject Matter***

Claims 4-7,9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-17 are allowed.

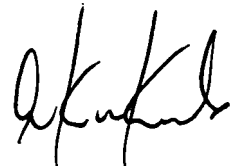
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arnold Kinkead whose telephone number is 571-272-1763. The examiner can normally be reached on Hoteling.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arnold Kinhead  
08-16-07

  
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